5300 series
Combinational Testers

Combinational testers offering multi-strategy solutions to handle the simplest through to the most complex test requirements

COMBINATIONAL TESTERS

- Analog and digital functional
- Analog and digital In-Circuit
- Reverse trace diagnostics
- Windows NT operating system
- Automatic program generation software
- Graphical program debug capability
- ISDN and Telecoms capability
- Inductive and capacitive vectorless test

Introduction

Traditionally, a single strategy tester was adequate to test the majority of conventional printed circuit boards. However, advances in technology and demands on board real estate necessitate a multi-strategy approach to ensure that the required level of fault coverage is maintained. This multi-strategy approach is achieved by the combinational tester, offering a wide range of test methods including In-Circuit, functional, boundary scan and a wide range of specialized techniques. Using this type of tester, the challenges presented by today's boards can be overcome.

Analog and digital In-Circuit test provides rapid program generation and accurate fault diagnosis, eliminating a wide spectrum of manufacturing faults. Alternatively, analog and digital functional testing detects dynamic faults and provides a high degree of confidence that the board will operate as the designer intended in the working environment.

The 5300 series provides two combinational platforms suitable for a wide range of applications throughout manufacturing test. They use a range of plug-in test card resources to reflect a multi-strategy test approach.

Architecture

The kernel of an ATE system is the card-cage which accomodates the plug-in test card resources and power supplies. Within the 5300 series, there are two systems offering two distinct styles of card-cage:

5305

A compact benchtop unit which has 14 slots within the card-cage for inclusion of test resources. The system can easily be mounted within a 19 in rack.

5300

A benchtop unit with a 21 slot capacity.

The test resources can be configured in a wide variety of combinations to provide the functionality required. Each card resource has it's own connector for interfacing to test fixtures, optimizing wire lengths and maintaining signal integrity.

Both systems use a industry standard Pentium based PC acting as a system controller. System software runs under the Windows NT operating systems, providing a high level of familiarity to users.

System Software

A range of software is available to meet the varied requirements of the different test methods found within the 5300 series combinational systems. To provide test programs, a Computer Aided Program Generation (CAPG) package takes CAD data to produce test programs and fixture build data. Within the program debug environment a range of graphical tools are provided to quickly and accurately commission tests. Further extensions are available to support such methods as boundary scan.

Test Methods

Each system within the 5300 series range is capable of accepting the full range of test resources. From an In-Circuit perspective, each system can be configured for analog and/or digital testing. For functional test, a wide range of stimulus and measurement cards can be fitted, enabling both analog and digital testing. The inclusion of a GPIB/VXI card within the system controller further enhances this range of tests to include commercially available instruments.

There are also dedicated cards for the testing of specific applications such as telecommunications and ISDN protocols. These can be mixed and matched with all of the other cards to maximize test coverage.

Program Generation Guide

http://www.ifrinternational.com
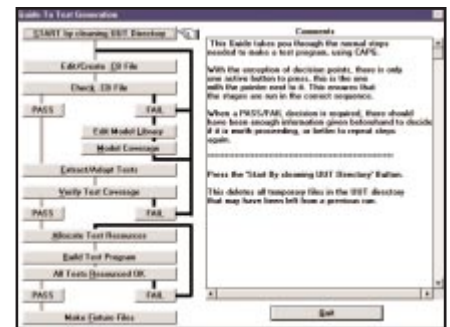
5300 series

Fixturing

The test subject is usually connected to the tester via a bed of nails vacuum or pneumatic fixture, routing each probe to a test resource within the system. For In-Circuit testing, providing access is available, it is usual to place a probe on each electrical node present within the circuit. In the case of functional test it is common to use fewer probes, allocated to the edge connectors.

Future Proofing

The modularity of the 5300 series combinational test systems makes them highly configurable. Although the initial requirement normally specifies the functionality of the tester, the modular approach allows for future changes and extensions of role. It is not uncommon to see a 5300 series tester configured several years after purchase to enable a completely different test philosophy.
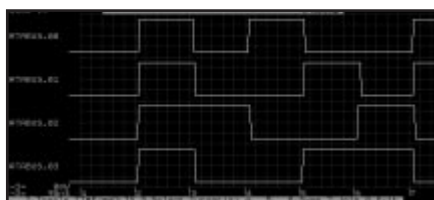
Digital Debugging Tool

Specification

GENERAL SYSTEM

Controller	Pentium PC
Software	Windows NT
User controls	Keyboard and footswitch input.
Test fixturing	Bed-of-nails or plain platten.

UUT POWER SUPPLIES

5305	
Standard	5 V, 10 A DC fixed supply.
Optional	Dual 0-30 V, programmable supply, current limit 2A.
5300	
Standard	5 V, 10 A DC fixed supply.
Dual	0-30 V, 45 W (5 A max), programmable supply.

CONDITIONS OF OPERATION WITHIN SPECIFICATION

Temperature	10°C to 35°C.
Humidity	20% to 75% RH (non-condensing).

CONDITIONS OF STORAGE & TRANSPORT

Temperature	–25°C to +70°C.
Humidity	0% to 95% RH (non-condensing).

POWER REQUIREMENTS

AC Supply Single phase AC supply, 198 V to 264 V or 99 V to 132 V, 47 Hz to 63 Hz.

DIMENSIONS & WEIGHT

(Testframe only, i.e. excludes PC controller)

5305

Height	Width	Depth	Weight
344 mm	534 mm	500 mm	38 kg

(Typical and configuration dependent)

5300

Height	Width	Depth	Weight
375 mm	927 mm	343 mm	75 kg

(Typical and configuration dependent)

ANALOG IN-CIRCUIT TEST (AIC) FACILITY

A comprehensive, fast analog in-circuit test option providing full 6-wire measurement capability for testing the most complex circuit networks on printed circuit boards.

The analog in-circuit test facility is a multi-card configuration which uses the following cards.

· In-Circuit Measurement & Stimulus Card (IMS)
· Serial Digital Controller Card (SDC)
· In-Circuit Relay Card (ICR96)

The AIC option features the following capability.

· 1200 components/s test speed
· Power on test
· Unique graphical program debug
· Auto program generation software
· Up to 1824 test pins
· Inductive and capacitive vectorless test

The AIC test resource is a fast analog in-circuit test facility which combines high speed test, the ability to test a wide range of component types and ease of use. It is supported by auto program and manual entry program generation. The test resource provides economic test facilities for high speed component test and accurate manufacturing defects identification.

Vectorless Test Capability

IFR Limited is unique in offering both inductive and capacitive vectorless techniques, ensuring wide test coverage across a range of components from complex ASICs to connectors. Inductive probing is performed using the IFR patented Q-test II technique, whilst capacitive tests use the industry standard HP TestJet™ probe. These two techniques contribute to the systems ability to generate tests for complex devices quickly, and to accurately diagnose faults to enhance productivity and quality.

Power-on Test Techniques

Using power-on test techniques means the AIC is able to test devices such as operational amplifiers as well as the traditional range of analog passive components including fuses and links.

Auto Program Generation

The AIC is supported by an auto program generation software package which permits fast, high quality test program generation. This auto program generation software minimizes test program development / commissioning times and speeds the product time-to-market sequence. Data can be input from CAD, netlists or keyed in manually.

Contact Test

Contact test is a high speed test fixture to unit-under-test contact verifier. The contact 'map' can be learned and saved to a file. This file can be edited to add or ignore pins. The learned data can be used

as a reference thereafter.

Test Point Search

Test point search is a test fixture debugging facility for verifying correct wiring or detecting which test pins are connected to a particular node on the unit under test.

Graphical Program Commission/Debug

A unique, graphical commissioning /debug facility provides the AIC with a powerful yet simple to use test program debug environment minimizing program commissioning times. The test block commissioning display identifies all components, by type, within the test program. Facilities for component block selection, the ability to run individual blocks, all program blocks, data logging control and access to the commissioning / debug facility are all controlled by simple selections.

The component test debugging facility provides 'point & click' access for editing component values, upper / lower limits, test and sense points, guards, delays, test and mode options. Also included within this environment is the graphical component debug tool. This interactive tool provides a graphical display of test results allowing the user to determine the stability and accuracy of the measurement.

Users can modify device measurement conditions and quickly see the effect on the stability of the measurement. The effects of filtering, averaging, measurement configuration and guard placement on a component test can be assessed virtually instantaneously. The facility allows users to optimize test speeds by allowing the user to reduce the delay on stable measurements until the measurement collapses. The optimum delay value is then displayed on a graphical plot. These comprehensive test program debug software tools minimize test program commissioning and debug times.

Component Failure Identification

This facility provides a graphical representation of the unit under test (UUT). The facility is user selectable and provides a visual identification of the position on the UUT of the failed or defective component. A selection of user controls are provided with the facility.

In-Circuit Check Card

An in-circuit check (ICC) card is provided with the AIC test resource for the 5300 and 5305. This allows the user to perform confidence checks on the stimulus and measurement facilities of the system. In addition test programs for the ICC card are provided with the AIC / system software which permits users to quickly become familiar with the system. The AIC user documentation package includes a user guide which is based on the ICC card as well as comprehensive hardware and software reference manuals.

Specification

Test Points
5300: up to 1824
5305: up to 1152

Component test
Up to 1200 components / s speed

Capacitor Discharge Voltage Monitor
Constant current,
200 mA limited, 30 V

Continuity (Shorts & Opens)

Stimulus level	200 mV
Threshold	10 Ω (default), 100 Ω or programmable

DC Voltage

Ranges	10 mV - 100 mV
	100 mV - 1 V
	1 V - 10 V
	10 V - 50 V
Input impedance	10 MΩ

DC Current

Ranges	0 -100 nA
	100 nA - 1 μA
	1 μA - 10 μA
	10 μA - 100 μA
	100 μA - 1 mA
	1 mA - 10 mA
	10 mA - 100 mA

Resistance (2/3 Wire)

Ranges	0.2 Ω - 2 Ω
	2 Ω - 20 Ω
	20 Ω - 200 Ω
	200 Ω - 2 kΩ
	2 kΩ - 20 kΩ
	20 kΩ - 200 kΩ
	200 kΩ - 2 MΩ
	2 MΩ - 20 MΩ
Stimulus level	0.2 Ω - 2 Ω range, 20 mV / 200 mA
All other ranges	200 mV / 200 mA

Resistance (4/6 Wire)

Ranges	0.2 Ω - 2 Ω
	2 Ω - 20 Ω
	20 Ω - 200 Ω
	200 Ω - 2 kΩ
	2 kΩ - 20 kΩ
	20 kΩ - 200 kΩ
	200 kΩ - 2 MΩ
	2 MΩ - 20 MΩ
Stimulus level	0.2 Ω - 2 Ω range. 20 mV / 200 mA
All other ranges	200 mV / 200 mA

Resistance (Extended 2/3 Wire)

Ranges:	200 kΩ - 2 MΩ
	2 MΩ - 20 MΩ
	20 MΩ - 200 MΩ
Stimulus level:	All ranges, 2 V / 200 mA

Resistance (Extended 4/6 Wire)

Ranges	200 kΩ - 2 MΩ
	2 MΩ - 20 MΩ
	20 MΩ - 200 MΩ
Stimulus level	All ranges, 2 V / 200 mA

Capacitance (2/3 Wire)

Ranges	2 pF - 20 pF
	20 pF - 200 pF
	200 pF - 2 nF
	2 nF - 20 nF
	20 nF - 200 nF
	200 nF - 2 μF
	2 μF - 20 μF
	20 μF - 200 μF
	200 μF - 2000 μF
Stimulus level	2 pF - 200 pF (2 ranges), 300 mV pk-pk / 200 mA
	200 pF - 2 μF (4 ranges), 120 mV pk-pk / 200 mA
	2 μF - 2000 μF (3 ranges), 50 mV pk-pk / 200 mA
Stimulus frequency	2 pF - 200 pF (2 ranges), 5.2 kHz
	200 pF - 2 μF (4 ranges), 1.3 kHz
	2 μF - 2000 μF (3 ranges), 325 Hz

Capacitance (4/6 Wire)

Ranges	2 pF - 20 pF
	20 pF - 200 pF
	200 pF - 2 nF
	2 nF - 20 nF
	20 nF - 200 nF
	200 nF - 2 μF
	2 μF - 20 μF
	20 μF - 200 μF
	200 μF - 2000 μF
Stimulus level	2 pF - 200 pF (2 ranges), 300 mV pk-pk / 200 mA
	200 pF - 2 μF (4 ranges), 120 mV pk-pk / 200 mA
	2 μF - 2000 μF (3 ranges), 50 mV pk-pk / 200 mA
Stimulus frequency	2 pF - 200 pF (2 ranges), 5.2 kHz
	200 pF - 2 μF (4 ranges), 1.3 kHz
	2 μF - 2000 μF (3 ranges), 325 Hz

Inductance (2/3 Wire)

Ranges:	20 μH - 200 μH
	200 μH - 2 mH
	2 mH - 20 mH
	20 mH - 200 mH
	200 mH - 2 H
	2 H - 20 H
	20 H - 200 H
Stimulus level	20 μH - 200 mH (4 ranges), 260 mVpk-pk / 200 mA
	200 mH - 200 H (3 ranges), 160 mVpk-pk / 200 mA
Stimulus frequency	20 μH - 200 mH (4 ranges), 5.2 kHz
	200 mH - 200 H (3 ranges), 1.3 kHz

Inductance (4/6 Wire)

Ranges	20 μH - 200 μH
	200 μH - 2 mH
	2 mH - 20 mH
	20 mH - 200 mH
	200 mH - 2 H
	2H - 20 H
	20 H - 200 H
Stimulus level	20 μH - 200 mH (4 ranges), 260 mVpk-pk / 200 mA
	200 mH - 200 H (3 ranges), 160 mVpk-pk / 200 mA
Stimulus frequency	20 μH - 200 mH (4 ranges), 5.2 kHz
	200 mH - 200 H (3 ranges), 1.3 kHz

Impedance (2/3 Wire)

(Unresolved Z)

Ranges:	0.2 Ω - 2 Ω
	2 Ω - 20 Ω
	20 Ω - 200 Ω
	200 Ω - 2 kΩ
	2 kΩ - 20 kΩ
	20 kΩ - 200 kΩ
	200 kΩ - 2 MΩ
	2 MΩ - 20 MΩ
Stimulus level	0.2 Ω - 2 Ω range, 40 mVpk-pk / 200 mA
All other ranges	400 mVpk-pk / 200 mA
Stimulus frequency	Programmable 0 - 50 kHz

Impedance (4/6 Wire)

(Unresolved Z)

Ranges	0.2 Ω - 2 Ω
	2 Ω - 20 Ω
	20 Ω - 200 Ω
	200 Ω - 2 kΩ
	2 kΩ - 20 kΩ
	20 kΩ - 200 kΩ
	200 kΩ - 2 MΩ
	2 MΩ - 20 MΩ
Stimulus level	0.2 Ω - 2 Ω range, 40 mVpk-pk / 200 mA
All other ranges	400 mVpk-pk / 200 mA
Stimulus frequency	Programmable 0 - 50 kHz

Impedance (2/3 Wire)

(Resolved Z)

Ranges:	0.2 Ω - 2 Ω
	2 Ω - 20 Ω
	20 Ω - 200 Ω
	200 Ω - 2 kΩ
	20 kΩ - 200 kΩ
	200 kΩ - 2 MΩ
	2 MΩ - 20 MΩ
Stimulus level	0.2 Ω - 2 Ω range, 40 mVpk-pk / 200 mA
All other ranges	400 mVpk-pk / 200 mA
Stimulus frequency	Programmable 0 - 50 kHz

Impedance (4/6 Wire)

(Resolved Z)

Ranges	0.2 Ω - 2 Ω
	2 Ω - 20 Ω
	20 Ω - 200 Ω
	200 Ω - 2 kΩ
	2 kΩ - 20 kΩ
	20 kΩ - 200 kΩ
	200 kΩ - 2 MΩ
	2 MΩ- 20 MΩ
Stimulus level:	0.2 Ω - 2 Ω range, 40 mVpk-pk / 200 mA
All other ranges	400 mVpk-pk / 200 mA
Stimulus frequency	Programmable 0 - 50 kHz

Diode Tests

Test modes	Diode forward voltage measurement (Diode 'ON'), Diode reverse test (Diode 'OFF') Diode leakage measurement
Current source	Up to 200 mA
Compliance voltage	Up to 30 V

Zener Diodes
Voltage measurement 1 V to 54 V

Transistor Tests

Test modes	Transistor on test (minimum gain), transistor off test & transistor leakage measurement (i.e. emitter - base and collector - base)
Base drive	Current range 0 - 200 mA
Collector drive	Compliance voltage 5 V

Other Components
FETs, transformers, electrolytic capacitors, relays, op-amps, opto-isolators, thermisters, fuses, links, SCRs, varistors.

Stimulus
Two stimulus channels which can be either DC or AC, independent of each other.

DC	-10 V to +20 V, four quadrant, programmable 0 - 200 mA, programmable, source or sink
AC	0 to 4 V pk-pk, programmable Programmable DC offset, -10 V to +10 V 0 - 200 mA, programmable, source or sink Frequency range, 0 to 100 kHz

In addition a DC source with a compliance voltage of up to 54 V (current limited) is available for testing Zener diodes.

UNIVERSAL IN-CIRCUIT TEST FACILITY

■ Analog In-Circuit

■ Digital In-Circuit

■ Digital Functional

■ Vectorless Test

A high performance facility providing the fault isolation benefits of in-circuit test combined with the dynamic capabilities of functional test.

The Universal In-Circuit (UIC) test option integrates both digital/analog in-circuit and functional test hardware and software into a single facility within the ATE system. Computer assisted program generation facilities supported by a comprehensive device library provide the ease of programming and fault detection benefits of in-circuit test. The UIC facility is further supported by sophisticated test program debug tools including the system's unique

5300 series

TruView™ software debug tool. The UIC test suite comprises the following card types:

- Control & Sequencer Card (CAS2)
- Resistance, Continuity & Control Card (RCC4)
- Capacitance, Inductance & Impedance Card (CLZ)
- Dual Voltage Source Card (DVS)
- Drive/Sense Card fitted with the Universal Test Pin Daughter Card (DAS/UTP).

A CAS, RCC4, CLZ and DVS card is required per system and up to 17 DAS/UTP cards may be fitted.

MODES OF OPERATION

The UIC facility has two modes of operation.

In-Circuit Test Mode

Primarily for the detection of connectivity, manufacturing and component faults, this mode provides facilities for testing both digital and analog devices and board tracking.

Functional In-Circuit Test Mode

This mode of operation provides a dynamic, digital functional facility with a test pattern rate of 10 MHz. In this mode the full facilities of the ATE's Digital Test System option are available with maximum pulse widths of 60 ns with edge plane to 20 ns.

BACKDRIVING TIMEOUT & RELAXATION FACILITIES

To prevent overheating of sensitive devices due to prolonged backdriving, the standard system software contains facilities to control timeout and relaxation hardware. The UIC test facility can be set to provide a test program timeout and to tristate the pinface in the event of a test program execution exceeding the timeout period. The relaxation facility is used to limit the test/no test ratio to prevent overstressing. In addition to being able to program the duration of the backdriving current, the backdrive duty cycle can also be programmed.

TEST PROGRAMMING & SOFTWARE DEBUG TOOLS

In addition to the standard system software which provides the facilities for programming all aspects of the UIC test capability, a range of sophisticated test programming and program debug tools are provided.

Computer Assisted Program Generation

Computer Assisted Program Generation (CAPG), is a computer assisted program generation software package and is supported by a comprehensive device library. Facilities for digital and analog network analysis, dynamic guarding and pin allocation are provided by CAPG. To minimise back-driving requirements CAPG will automatically allocate static and/or dynamic guards as required.

TruView

TruView is a real-time debugging tool with an effective bandwidth of 300 MHz. It eliminates the need for external instrumentation, interconnection probes, special pods and additional fixture wiring when commissioning in-circuit or functional test programs. TruView's 800 MHz equivalent time sampling capability operating independently on every test pin, enables a true display of nodal activity, timing and analog behaviour of stimulus/response signals. Four display modes are provided.

Vectorless Test Capability

IFR Limited is unique in offering both inductive and capacitive vectorless techniques, ensuring wide test coverage across a range of components from complex ASICs to connectors. Inductive probing is performed using the IFR patented Q-test II technique, whilst capacitive tests use the industry standard HP TestJet™ probe. These two techniques contribute to the systems ability to generate tests for complex devices quickly, and to accurately diagnose faults to enhance productivity and quality.
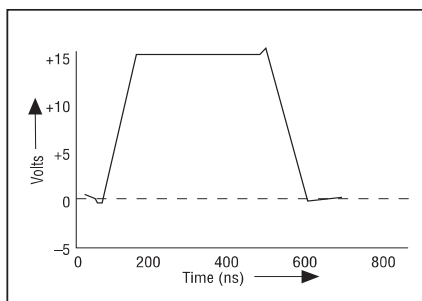
Typical DAS/UTPHV Waveform

Contact Test

Contact test is a high speed test fixture to unit-under-test contact verifier. The contact 'map' can be learned and saved to a file. This file can be edited to add or ignore pins. The learned data can be used as a reference thereafter.

Test Point Search

Test point search is a test fixture debugging facility for verifying correct wiring or detecting which test pins are connected to a particular node on the unit-under-test.

Bugprobe

Bugprobe is a facility which detects whether or not device pins are making contact with the unit-under-test board tracks. Running this option generates a graphical representation of the device. Initially all pins on the device displayed appear as filled blocks. When a pin is probed, which is making contact with the unit-under-test board track, the display changes to an outline block and if no contact is made the display remains a filled block.

Specification

Digital In-Circuit Testing

Test points	Up to 1088 (384 on 5305) 64 per DAS/UTP card multiplexed 1:4.
Pattern rate	10 MHz maximum.
Test rate	Average 15 components per second.
Pinface drive & sense skew	Typically 25 ns.
Timing resolution	20 ns.
Backdrive time	400 µs default, user programmable 192 µs to 65 ms with automatic relaxation and timeout facilities.

Guarding

Static	All pins, selectable High or Low.
Dynamic	Allocated automatically by CAPG.

Drivers

Voltage	Programmable drive high and drive low.
Range	±5 V.
Resolution	39 mV.
Accuracy	±200 mV.
Driver current	750 mA source, 500 mA sink, current limited.
Driver voltage	Programmable drive high and drive low.
Slew rate	150 V/µs, ±10%.

Sensors

Threshold	Dual.
Range	–5 V to +4.961 V.
Resolution	39 mV.
Accuracy	±200 mV.
Sensor voltage	Programmable sense high and low per 64 pin card.
Detection	High, Lo or Tristate.

Analog In-Circuit Testing

Test points	Up to 1088 (384 on 5305) 64 per DAS/UTP card.
Test rate	Average 30 components per second.

Capacitor Discharge

Capacitor range	Up to 10,000 µF max.
Discharge time	4 ms/10 µF.

Continuity (Shorts & Opens)

Stimulus level	100 mV.
Threshold	5 Ω, 10 Ω, 20 Ω, 50 Ω or 100 Ω. (selectable)

DC Voltage

Ranges	0 V to 100 mV.
	100 mV to 1 V.
	1 V to 10 V.
	10 V to 50 V.
Accuracy	±0.3% to ±1.5%.*
Input impedance	10 MΩ.

DC Current

Ranges	0 to 100 nA.
	100 nA to 1 µA.
	1 µA to 10 µA.
	10 µA to 100 µA.
	100 µA to 1 mA.
	1 mA to 10 mA.
Accuracy	±1% to ±2% .*

Resistance (DC)

Stimulus level	≤ 100 mV.
Ranges	1 Ω to 10 Ω.
(2 &4-terminal)	10 Ω to 100 Ω.
	100 Ω to 1 kΩ.
	1 kΩ to 10 kΩ.
	10 kΩ to 100 kΩ.
	100 kΩ to 1 MΩ.
	1 MΩ to 10 MΩ.
Accuracy	±1% to ±2%.*

Resistance (DC extended range)

Stimulus level	≤1 V.
Ranges	100 Ω to 1 kΩ.
(2 & 4-terminal)	1 kΩ to 10 kΩ.
	10 kΩ to 100 kΩ.
	100 kΩ to 1 MΩ.
	1 MΩ to 10 MΩ.
	10 MΩ to 100 MΩ.
Accuracy	±1% to ±2%.* (10 MΩ to 100 MΩ range accuracy unspecified)

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Resistance (AC)

Stimulus level	≤100 mV rms.
Stimulus frequency	100 Hz, 1 kHz & 10 kHz.
Ranges	16 Ω to 160 Ω.
(2 & 4-terminal)	160 Ω to 1.6 kΩ.
	1.6 kΩ to 16 kΩ.
	16 kΩ to 160 kΩ.
Accuracy	±3%.
	(16 kΩ to 160 kΩ range, accuracy unspecified if 1 kHz or 10 kHz stimulus used)

Capacitance

Stimulus level	≤100 mV rms.
Stimulus frequency	100 Hz, 1 kHz & 10 kHz.
Ranges	20 pF to 1 nF.
(2 & 4-terminal)	1 nF to 10 nF.
	10 nF to 100 nF.
	100 nF to 1 mF.
	1 mF to 10 mF.
	10 mF to 100 mF.
	100 mF to 1000 mF.
Accuracy 2-terminal	±5 pF ±(2% to 3.5%) †.
accuracy	(100 mF to 1000 mF range, unspecified)
Accuracy 4-terminal	±2%.
	(20 pF to 10 nF ranges, accuracy unspecified)

Inductance

Stimulus level	≤100 mV rms.
Stimulus frequency	100 Hz, 1 kHz & 10 kHz.
Ranges	25 µH to 250 µH.
(2 & 4-terminal)	250 µH to 2.5 mH.
	2.5 mH to 25 mH.
	25 mH to 250 mH.
	250 mH to 2.5 H.
	2.5 H to 25 H.
Accuracy 2-terminal	±4%.
	(25 mH to 250 mH range, accuracy unspecified)
Accuracy 4-terminal	±4%.
	(250 µH to 25 µH ranges, accuracy unspecified)

Impedance

Stimulus level	≤100 mV rms.
Stimulus frequency	100 Hz, 1 kHz & 10 kHz.
Ranges	16 Ω to 160 Ω.
(2 & 4-terminal)	160 Ω to 1.6 kΩ.
	1.6 kΩ to 16 kΩ.
	16 kΩ to 160 kΩ.
Accuracy	±5%.
	(Accuracy dependent on complex impedance under measurement)

Diode Tests

Diode forward voltage measurement (Diode 'ON').
Diode reverse test (Diode 'OFF').
Diode leakage measurement.

Current source	Up to 25 mA.
Compliance voltage	Up to 25 V.
Zener diodes	1 V to 24.6 V.

Transistor Tests

Transistor on test (Minimum gain).
Transistor off test.
Transistor leakage measurement
(i.e. emitter to base and collector to base).

Base drive	Current range 0.25 mA to 8 mA.
Collector drive	Compliance voltage 5 V.

* Dependent on range and test mode
† Dependent on range
System Residual Impedance.
series resistance, +2 Ω±1 Ω.
series inductance, +3 µH±2 µH.
Shunt capacitance, ±5 pF (2-wire), +40 pF±30 pF (4-wire).

BOUNDARY SCAN

- ■ Stand-alone device testing
- ■ Full scan path capability
- ■ Virtual In-Circuit option
- ■ Fully integrated into program generation software

A range of cards and software providing rapid test generation for PCBs with boundary scan implemented.

Boundary Scan Overview

The increasing use of high density complex surface mount devices, coupled with the reduction in nodal access has resulted in an increase in test development costs. The need to provide alternate methods of test access resulted in the adoption of the IEEE 1149.1 standard which defines the boundary scan architecture.

Boundary scan permits access to a device via four dedicated pins known as the Test Access Port (TAP). This TAP can be used for the testing of an individual device or, through daisy-chaining, a group of devices connected together.

Test Strategies

A typical boundary scan test strategy often has six elements associated with it :

- boundary scan path integrity check
- device identification check (IDCODE)
- interconnect tests
- device internal tests (INTEST)
- device built-in self test (BIST)
- external tests (EXTEST)

Scan Software

Each device supporting boundary scan has an associated Boundary Scan Description Language (BSDL) file. This file defines the extent of the boundary scan test strategies supported and the physical characteristics of the TAP element of the device.

'Virtual In-Circuit'

Where devices with and without the boundary scan capability are mixed together, a technique known as Virtual In-Circuit provides a high level of fault coverage to areas which were previously untestable. This technique requires an In-Circuit capability and the embedding of boundary scan test code within the test program generation software.

Boundary Scan Card Options

The 5300 series boundary scan facility consists of two dedicated cards and associated software. Single devices featuring a TAP can be tested using a single card, Virtual In-Circuit requires additional Universal In-Circuit cards to be fitted within the system.

The Boundary Scan Card (BSC) provides a solution to most boundary scan requirements, offering the following features :

- Three isolated boundary scan channels per card for multiple scan chains.
- Multiple external and internal clock, trigger and handshake facilities.
- 48 parallel, bi-directional I/O lines for stand alone testing of individual devices.
- Synchronization to the Universal In-Circuit option for high speed mixed mode testing.
- Full isolation of all interface signals for combined In-Circuit operation.

The Boundary Scan Input/Output card (BSIO) extends the capability of the BSC card by providing 77 additional bi-directional digital I/O channels.

Test Programs

The 5300 series boundary scan software enables the user to perform standard EXTEST, INTEST, BYPASS and SAMPLE modes. Special device specific options are can also be supported by the software. Test programs are generated using CAD information and individual BSDL files within the Computer Assisted Program Generation (CAPG) software used by all 5300 series testers. Two levels of software are provided, supporting basic stand alone boundary scan or a fully integrated Virtual In-Circuit capability.

The program generation software includes all of the executable code required to perform the boundary scan tests, and handles the necessary testpoint allocation. This facility permits the detection of 100% of pin-level faults including stuck-at-1, stuck-at-0, broken bond wires, shorts and incorrect or missing components. No probing is required and clear diagnostic messages are automatically provided by the test system.

5300 series Boundary Scan Options

- Level 1 CAPG Boundary Scan software,
- Level 2 CAPG Boundary Scan software
- Boundary Scan Card (BSC)
- Boundary Scan Input/Output Card (BSIO).

DIGITAL FUNCTIONAL

- ■ Digital Functional Testing
- ■ Conditional/Unconditional Branching
- ■ Algorithmic Pin Control micro-instructions

Digital Test System (DTS)

A 10 MHz, dynamic digital test facility capable of providing economic solutions to complex test requirements.

The architecture (APC-SLICE™) of the DTS option provides 10 MHz, dynamic digital test capabilities. One DTS control card is required to support up to 20 DTS stimulus/response cards providing up to 320 digital test channels. The micro-program controller on the DTS control card can change program flow in real time depending on UUT events and control the execution of Algorithmic Pin Control micro-instructions.

The DTS controls timing set selection, sampling mode selection, results logging, start/stop control of CRC registers, sequencing of APC-SLICES and external synchronizing facilities.

Each DTS stimulus/response card provides 16 individually controllable, protected drive-sense channels, a 2 x 64-bit APC microcode memory and a 16-bit APC-SLICE. Hardware support on a per

channel basis is also implemented for data formatting, signature analysis, pattern recognition, results logging, pinface deskew, isolation and switchback relays.

Data compression and re-usable test vector techniques coupled with fast, flexible pattern generators enable the DTS to store 'test instructions' as opposed to actual test patterns. This means that the APC-SLICE architecture requires much less high speed RAM behind each digital test channel compared with traditional architectures.

Dynamic timing facilities are provided through the use of timing sets and data formatting techniques. Timing information is derived from a timing set generator and 'overlayed' on the APC test patterns by the data formatter. Variable length timing sets, incorporating selectable 'on-the-fly' facilities enable the DTS to switch between emulating a Write test cycle and a Read test cycle dynamically.

An extensive range of software commands allow conditional/unconditional branching, looping and subroutine calling within the test patterns at full test rate.

Specification

TIMING

Reference clock	50 MHz.
Sub-cycle	20 ns, or n x 40 ns, or n x 500 ns
interval	(n = 1, 2, 3, ..., 16).
Main-cycle	n x sub-cycle interval
Interval	(n = 5, 6, 7, ..., 64).
External frequency/ clock inputs	50 MHz maximum, TTL,/ either or both edges.
External clock divider	1, 2, 3, ..., 16. (Maximum single step rate is 6.67 MHz or 3.33 MHz if using both edges.)
External clock delay	0 to 245 ns in 5 ns increments.
External sync	By use of external clock/frequency inputs. Test rate max.10 million patterns per second (unformatted, unmultiplexed).
UUT timing	9 lines : 4 Keep alive Clock output Handshake acknowledge Keep alive 1 Keep alive 2 5 Hold User timing lines.
Drive or sense phases	4 variable length timing sets (selectable 'on-the-fly') with 6 timing phases per timing set. Selectable per pin, giving edge placement of drive and sense windows to 20 ns resolution.
Sensor strobe	Programmable in sub-cycle steps (20 ns resolution).
Wait Flag	Active flag holds DTS and UT1-UT5 timing signals; CLOCK, ACK and KA1, KA2 signals continue. Active position of flag controlled to within 20 ns.

MICROPROGRAM CONTROLLER

Microprogram memory	4K steps.
Control commands	DELAY n as integer (231-1) REPEAT n/ENDREPEAT, LOOP n/ENDLOOP, JUMP_TO, CALL/RETURN, STOP, WAIT_FOR_HANDSHAKE.
Control condition	UNCONDITIONAL, NEVER, IF_FAULT, IF_NO_FAULT, IF_CHECK_PASS, IF_CHECK_FAIL, IF_EXTERNAL_HI, IF_EXTERNAL_LO, IF_HANDSHAKE_PRESENT, IF_NO_HANDSHAKE, Register Condition.
User Registers	8 (General purpose or address registers).

16-bit APC-SLICE

APC microcode memory	2K x 64 bits with data compression, reusable instructions and individual tristate control per pin.
APC configurations	1 to 320 APC pins (in 16-bit slices).
APC pattern instructions	INCREMENT, DECREMENT LOGICAL, ARITHMETIC, SHIFT etc.
APC instructions	DMH (Drive and Monitor HI), DML (Drive and Monitor LO), DRH (Drive HI), DRL (Drive LO), MNH (Monitor HI), MNL(Monitor LO), MNZ (Monitor Tristate) *, INH (Inhibit), SDH (Simulation Drive HI), SDL (Simulation Drive LO), SMH (Simulation Monitor High), SML (Simulation Monitor LO), SMZ (Simulation Monitor Tristate) *, TOG (Toggle), KEE (Keep) * Not available TTL/+5 V CMOS daughter card.
Effective test vector depth	Typically 4K for SRC and simulation modes, virtually unlimited for functional modes.

DATA FORMATTER

Data formats	NRZ, DNRZ, RZ, R1, RI, RC.

PATTERN RECOGNISER

Test for logic high, low, tristate, mask

Sense modes	Edge, window, accumulate, open.

RESULTS LOGGER

4K deep per pin. (Log all results, failed tests, failed checks, or all failures.)

SIGNATURE ANALYZER

Separate, maskable 16-bit CRC register per pin.

AUTO PINFACE DESKEW

Per pin via the pinface. Any pin to any other pin, skew is ±5 ns.

DRIVERS/SENSORS

High speed TTL/+5 V CMOS daughter card.

Driver/sensor channels	16 bidirectional channels/DAS card up to max 320 (144 on M505).
Drive levels	TTL and 5 Volt CMOS compatible.
Sense levels	TTL compatible.
Drive current	Symmetrical ±10 mA.
Auxiliary monitors	16 channels to internal sensors or auxiliary buffered outputs.
Multiplexed outputs	16 channels multiplexed to two outputs - MUX A or MUX B.
Protection	Drive/sense overvoltage, −1 V to +6 V.
Isolation	Relay isolation per channel.
Switchback path	Switch back relay to pinface per channel.

For details of other daughter cards contact IFR Ltd.

OTHER FACILITIES

Programmable timeout	192 μs to 65535 μs in 64 ms steps to tristate the pinface after a programmed interval has elapsed.
Stop modes	Stop on end of test, or Stop on failed test, or Stop on failed monitor, or Stop on any failure. Plus option to tristate the pinface on failure or end of test.
Failure reporting	Display/print 'x' number of test failures after test 'y'.
Size of tests	Multiple compiled blocks allowed in one test program.
Compilation	Either compile during test or compile to disc i.e. 'source' may be optionally held in the program or externally.
Other outputs	Trigger & fail signals.
Other inputs	External handshake.

LOGIC ANALYZER

■ An instrument providing 100 MHz timing and 10 MHz state analysis across 64 channels.

The Logic Analyzer provides facilities for high performance timing and state analysis. It can be used in either the ATE or interactive display modes of operation. In the ATE mode all the setup and analysis functions are fully automated, effectively deskilling the instrument environment set-up. In the interactive mode the user is free to display and examine results on the tester's monitor.

Providing up to 64 channels with a 10 ns (100 MHz) sampling resolution it contains facilities for both timing and state analysis. Interactive timing/state measurements can be made using the cross linking facility between the trigger and acquisition sections of the logic analyzer cards. Asynchronous and sequential triggers, magnification, signal name allocation, cursors and trigger event markers are all provided as standard.

Specification

Inputs

Data	64.
Clock qualifier	8 channels; 1 clock & 7 qualifiers.
Ext. frequency	One channel.
Logic threshold	TTL.
Impedance	1 x TTL FAST load.
Setup time	Data to clock: 23 ns.
Qualifier to clock	30 ns.
Hold time	Zero.

Data Acquisition - Timing Analysis Mode

Internal Clock	
Sample rate	98 kHz to 100 MHz.
Sample interval	10 ns, 20 ns to 5120 ns in 20 ns steps. 5120 ns to 10240 ns in 40 ns steps.
No. of samples	1016.
External Frequency	
Sample rate	DC to 50 MHz.
No. of samples	1016.

Data Acquisition - State Analysis Mode

External Qualified Clock	
Sample rate	DC to 10 MHz.
Clock qualifier	8 channels, 1 clock & 7 qualifiers.
Edge	Positive or negative.
No. of samples	1016.

Trigger Control

Asynchronous Trigger	
Trigger word	64 bits, selectable 1, 0 or X in any combination with or without filter. Trigger on equal or not equal.
Filter	20 ns to 300 ns. Resolution, 20 ns. Accuracy, −0 ns/+30 ns.
Arm	Auto or manual.
Trigger delay	Linkage to delay modes.
Sequential Trigger	
No. of levels	250.

Trigger word	Find word A.
	Find word A B C ....Z.
	Find sequence A B C ....Z.
	Delay n cycles (n = 1 to 4095).
	Trigger on sequence break.
	Goto label.
	Goto label if word.
	Goto label if sequence.
	Trace on & off.
	Trigger.
Trigger delay	Linkage to delay modes.

Trigger Delay Modes

Time	Selectable from 40 ns to 667 ms.
Ext. frequency	0 to 65535 cycles.
Ext. qualified clock	0 to 65535 cycles.
Asynchronous trigger word event	0 to 65535 occurrences.
Sequential trigger events	0 to 65535 occurrences.
ATE events	0 to 65535 occurrences.

Trigger Position
Selectable from 4 to 1008 in steps of 4.

ACTIVE DIAGNOSTIC PROBE AND CARD

- Analog measurement & stimulus capability
- Captures digital signals for reverse trace diagnostics

A comprehensive diagnostic facility using reverse trace techniques for rapid fault location.

The Diagnostic Probe Card (DPC) can interface active or passive probes to capture digital signals and to source or measure analog voltages. Each DPC contains unique firmware providing recognition, status and self test capability.

The Diagnostic Probe Card Kit comprises:

- Diagnostic Probe Card (DPC)
- Reverse Trace Compiler Disc.

The Active Diagnostic Probe (ADP) is connected to the DPC card using a connector fitted to the rear of the card. The ADP provides direct and, via a X1 or a X10 range selection, buffered signal inputs. Three coloured LEDs on the ADP provide logic level and pulse indicators.

The DPC has both digital and analog resources to support probing functions on faulty printed circuit cards and features an optimizing reverse trace algorithm providing digital diagnostic back tracing facilities. This algorithm ensures that faulty nodes are identified with a minimum of probing actions. Analog facilities include DC and AC voltage measurement, positive and negative peak detection and switching to identify faults in the analog sections of printed circuit cards.

Digital Facilities

The DPC has the facility to capture nodal data, up to a depth of 64 k patterns, necessary for reverse trace activity. In addition it is able to perform CRCs on circuit activity. These facilities provide the benefits of accurate digital diagnostics on printed circuit cards containing complex designs involving, for example, digital feedback loops and bus controlled circuitry.

Nodal data can be learned from a known good UUT or imported from a digital simulator. During the learn, verify and diagnose phases, nodal data can be displayed in a logic analyzer style display for comparison with previously learned data. An error trace highlights differences between any two selected traces aiding both test program commissioning and fault finding. Any combination of node and test number can be masked by entering 'don't cares' (X's).

DIAGNOSTIC PROBE CARD – FUNCTIONAL BLOCK DIAGRAM
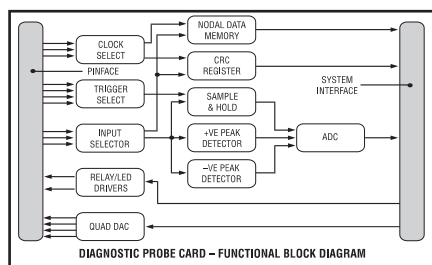
Analog Facilities

The following facilities are supported:

- DC and AC peak voltage measurement, ranges ±10 V and ±100 V.
- DC volts can be measured either under test program control or on an external trigger event utilizing the on-board sample and hold facilities. Four internal, four external hold trigger options and four arming options are available.
- External triggering facilities.
- Positive and negative peak voltage detection/measurement.
- Four independently programmable output voltages are available using the on-board quad DAC*.
- User/software controllable, general purpose relays for input signal routing.

Specification

Nodal Data Capture

Results Store	64 k x 2 RAM, linear.

CRC Capability

Register	16-bit CRC.

Digital Input

Level	TTL/5 V CMOS compatible.
Impedance	2 ACT loads.

Analog Input

Impedance	1 MΩ/50 pF.
Pull up	10 kΩ to programmable voltage using DAC1.

Voltage Measurement

Ranges	±10 V and ±100 V DC or AC peak
Accuracy	±0.5%full scale +(0.5% of reading).
Bandwidth	20 kHz.

Sample And Hold Facilities

Arming	Internal arming.
	Arm on an external edge, level, arm active (Software polling function).
Triggering Facilities	Internal trigger.

	Trigger on a digital test step, probe digital signal input. External trigger (Three sources). Inverted external trigger. Inverted external trigger.
External Control Signals	TTL compatible.
Measurement Accuracy	±0.5%full scale +(0.5% of reading).

Peak Detectors

Droop Rate	0.2 mV/ms.
Measurement Accuracy	±0.5%full scale +(0.5% of reading).

Digital To Analog Converter

| DAC 1	Output range ±10 V. Resolution 80 mV. Accuracy ±600 mV. Output current, 25 mA maximum.
DAC 2*,3* &4	Output range ±5 V. Resolution 40 mV. Accuracy ±100 mV. Output current, 25 mA maximum.

ADP Specification

Sensor range	±5 V (X1) & ±50 V (X10).
Sensor threshold resolution	40 mV (X1) & 400 mV (X10)
Sensor threshold accuracy	±100 V (X1) & ±[1 V + 2% of reading] (X10).
Sensor delay	–20 ns.
Input impedance	5 MΩ (X1) & 30 kΩ (X10).
Input capacitance	10 pF.
Input protection	±100 V.
Bandwidth	140 MHz.
Hysteresis	60 mV (X1) & 600 mV (X10).

Probe Skew (Skew figures using the ADP are relative to a 1.5 V threshold.)

Probe Type	Deskewed	Undeskewed
Passive	±5 ns	±10 ns
Active (ADP)	±5 ns	±15 ns

* DACs 2,3 and relay drivers not available when an active diagnostic probe is used.
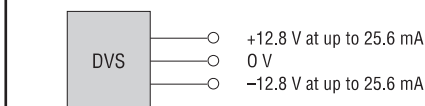
DUAL VOLTAGE SOURCE

Each source can be configured as:-

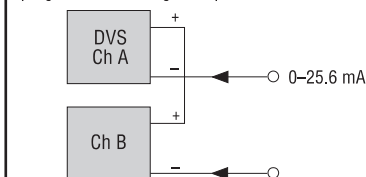Two-terminal floating source 0 V to 25.6 V

0 V to 25.6 V at up to 25.6 mA

or
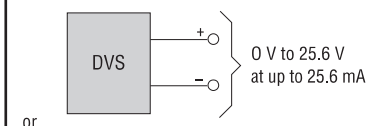
Three-terminal bipolar twin source. Twin tracking, with each rail capable supplying 0 V to ±12.8 V, with symmetry about the common rail.

+12.8 V at up to 25.6 mA
0 V
−12.8 V at up to 25.6 mA

or using both sources.

Floating programmable Current source with programmable voltage compliance.

0–25.6 mA

DVS Configurations

5300 series

■ A dual channel, fully floating, programmable source configurable to provide voltage stimuli or to operate as a current controller

The Dual Voltage Source (DVS) can be used as a programmable source or used in conjunction with the in-circuit test cards as an integral part of the dynamic, universal in-circuit test resource.

The DVS provides stimuli for functional testing, in-circuit active component testing and external instrumentation programming. It provides two sources per card, each completely isolated from both the system and user power supplies and the other channel.

Voltages of up to 25.6 V can be supplied or currents of up to 25.6 mA per source can be controlled. Each source can be configured as a programmable current controller or a voltage source.

Specification

Output
Dual output, voltage or current programmable.

DC Voltage Ranges (Full Scale)
1.28 V with 1.25 mV resolution (each source).
12.8 V with 12.5 mV resolution (each source).

Voltage Accuracy
±0.4% of demand, ±0.1% of range.

DC Current Range
25.6 mA each source with 25 mA resolution.

Current Accuracy
±0.6% of demand, ±0.1% of range.

Configurations
Each source can be configured as a two-terminal floating source (0 V to 25.6 V at up to 25.6 mA) or a three-terminal bipolar twin source, twin tracking, with each rail capable of supplying 0 V to 12.8 V with symmetry about the common rail.
Using both channels the DVS can be configured as a floating, programmable current source with programmable voltage compliance.

WAVEFORM SYNTHESIZER

■ A fully independent two channel, programmable instrument
■ Facilities to generate sine, square, triangle, pulse, ramp and user defined waveforms.

The Waveform Synthesizer Card (WSC) comprises two fully independent output channels with individually programmable waveform amplitude, offset, relay isolation and output protection. Fully independent gating and triggering facilities are provided for each channel. Frequency is crystal controlled using the internal clock or an external reference clock may be used.

Features

- Two fully independent channels per card.
- Sine, square, pulse, triangle and ramp outputs.
- Arbitrary/user generated waveforms.

- Fully independent trigger on each channel.
- Programmable phase shift/delay between channels.
- Single shot, multiple shot and continuous operation.
- Relay isolation and full output protection on true and complement outputs.
- Gain control (amplitude modulation) inputs.
- Channel A modulated by channel B via internal path.

The two channels provided by the WSC can be separately configured in one of four operating modes, each of which is optimized for the type of waveform to be generated.

PLL Mode

In this mode the WSC provides waveform generation facilities for varying types of waveforms. The phase shift between channels in PLL mode is dependent on the number of samples per cycle in the waveform. The phase shift can be any multiple of one sample.

DDS Mode

In DDS (direct digital synthesis) mode the WSC provides sine waveforms with frequency resolution of better than 1.25 MHz across the full frequency range of 1.25 MHz to 312.5 kHz. In this mode the initial phase shift is programmable in steps of less than 0.0125_.

PULSE mode

PULSE mode allows pulse widths to be stepped in 200 ns steps from 1 ms to 1 s. In PULSE mode the channels can be delayed relative to each other by 200 ns steps up to a maximum of 835 ms.

ARB MODE

This allows arbitrary waveforms to be generated from user supplied data files. In ARB mode the phase shift can be any multiple of one sample.

Specification

Analog Signals

Source impedance:	50 Ω ±5%.
AC amplitude:	0 V to 20 V peak-to-peak into an open circuit.
AC resolution:	8 bits (78 mV into an open circuit with gain control disabled).
DC amplitude:	−5 V to +5 V.
DC resolution:	8 bits (40 mV).
AC+DC accuracy:	±80 mV at 20 V peak-to-peak signal into an open circuit.
Output protection:	Relay isolated, all channels. Overvoltage protection to ±30 V DC. Short circuit and thermal overload protected. Automatic isolation of outputs in event of fault condition.
Gain control range:	0 V to −10 V. Scaling − 2 V peak-to- peak of AC waveform per control Volt, ±10%.
NOTE:	Control voltage must be offset by −10 V.

Digital (TTL) Signals

Master clock output:	1.2 MHz to 2.4 MHz in PLL mode, 2.5 MHz in DDS mode, 5 MHz in PULSE mode, 2.5 MHz in ARB mode and

	buffered external clock input.
External clock frequency input:	5 MHz max. (Actual frequency is mode dependent), duty cycle 50%, ±5%.
External trigger:	Positive edge controlled, single and multiple cycles, re-triggered single and multiple cycles.
External gate:	AC part of waveform disabled when pulled low.
NOTE:	All digital inputs are pulled up via 4.7 kΩ to +5 V).

Internal Timebase

Accuracy:	±100 ppm.

OPERATING MODES

PLL Mode
Frequency range (sine and square):
0.15 Hz to 300 kHz in 21 ranges.

Frequency range (triangle and ramp):
0.6 Hz to 300 kHz in 19 ranges.

Frequency ranges:
Range 1 – 150 kHz to 300 kHz,
Range 2 – 75 kHz to 150 kHz,
Range n – 1.2 MHz ÷ $2^{(n+2)}$ to 2.4 MHz ÷ $2^{(n+2)}$.

Frequency resolution:
Range 1 – 1 kHz,
Range 2 – 500 Hz,
Range n – 8 kHz ÷ $2^{(n+2)}$.

Harmonic Distortion (sine wave):
50 dB down.

Phase shift resolution:
Range 1 – 45_ [150 kHz to 300 kHz],
Range 2 – 22.5_ [75 kHz to 150 kHz],
Range n – 360_ ÷ $2^{(n+2)}$ [1.2 MHz ÷ $2^{(n+2)}$ to 2.4 MHz ÷ $2^{(n+2)}$].

NOTE:
Minimum phase resolution is 0.05_ for triangle and ramp and 0.0125_ for sine and square waveforms.

Master clock output:
1.2 MHz to 2.4 MHz in 8 kHz steps, phase locked to either internal or external 8 kHz reference.

NOTE:
Figures quoted for this mode assume default table length of 8192 samples and full scale output into a 50 Ω load.

DDS Mode

Frequency range:
1.25 MHz to 312.5 kHz.

Frequency resolution:
Better than 1.25 MHz.

Harmonic distortion:
Largest harmonic >50 dB down.

Phase shift:
0_ to 360_ in 0.0125_ steps.

NOTE:
Figures quoted for this mode assume default table length of 32768 samples and full scale output into a 50 Ω load.

PULSE Mode

Rise time:
250 ns.

Fall time:
250 ns.

Pulse width (mark or space):
1 ms to 835 μs.

Pulse repetition rate:
<1 Hz to 500 kHz.

Resolution:
200 ns.

Phase shift/delay:
Equivalent of 200 ns steps.

NOTE:

http://www.ifrinternational.com

Parameters quoted assume that an internal clock and a 50 Ω load are used.

ARB mode

Sample length:
5 samples to 8 k samples.

Master clock:
Internal – 2.5 MHz, external – 2.5 MHz maximum.

Sample clock frequency:
Integer divisions of master clock.

Waveform generation:
Using standard functions and WSC profiles.

ANALOG SAMPLING CARD

■ An instrument with embedded digital signal processing providing sampling oscilloscope, low frequency spectrum analysis, DVM and signal generation facilities.

The Analog Sampling Card (SAM[HR]) is a single channel instrument combining the functions of a sampling oscilloscope, low frequency spectrum analyzer, DVM and signal generator on a single card for applications requiring high accuracy measurements in the time and frequency domains over the range DC to 50 kHz. The card features on-board, 5 MHz digital signal processing and a 12-bit ADC to provide the following signal processing and measurement facilities.

Time Domain

Single value at reference cursor
RMS value of record data
Peak value at cursor position
Average, max. and min. peak value in record
Peak to peak value
Proximal (10%), Mesial (50%) & Distal (90%) values

Time Domain Trace Processing

Rise and fall times
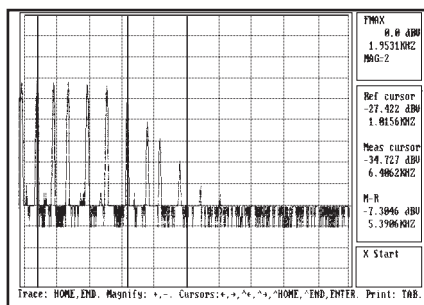
Analog Sampling Card Spectrum Analyzer Display

Mark duration
Space time
Period and frequency
Slope (positive and negative)
Pulse count
Cursor positioning
Proximal, Mesial and Distal occurrence time from trigger

Time Domain Trace Post Processing

Waveform mask testing (UL, LL envelope)
Add, subtract, multiply, square, square root and invert waveform
Convert waveform to dB
Fast Fourier Transform (FFT)
Discrete Fourier Transform (DFT)
Block floating point FFT
Load/save waveform to disk

Frequency Domain Trace Processing

Power spectrum calculation
Phase/magnitude spectrum
Window function selection
Frequency (reference cursor, measurement cursor)
Level (reference cursor, measurement cursor)
Test waveform against mask
Find peak level, frequency and width
Fundamental, harmonic and noise power
Count peaks in waveform
dB relative to reference level
dB relative to reference power level into specified termination

Frequency Domain Trace Post Processing

Add, subtract reference waveform
Multiply by reference waveform
Inverse transform (frequency to time domain)
Load/save waveform to disk

Specification

General

Number of channels: 1.
Inputs: Main (1), differential (1) and auxiliary (6).

Main Input

Input coupling: AC or DC, selectable.
Input impedance: 1 MΩ/25 pF.
Sensitivity: 100 mV full scale to 100 V full scale (10 divisions in 1-2-5 steps).
DC accuracy: 100, 200, 500 mV full scale - ±0.5% of reading ±0.25 mV. 1, 2, 5, 10, 20, 50, 100 V full scale - ±0.1% of reading ±0.1% of full scale range.
Resolution: 12-bits (0.024%) of full scale.
Position (DC offset): Adjustable over ±5 divisions with 12-bit resolution.
Maximum input voltage: 100 V (DC + AC peak).
Small signal bandwidth (–3 dB points): DC - 0 Hz to 425 kHz, AC - 1 Hz to 425 kHz.
Large signal bandwidth: DC - 0 Hz to 50 kHz, AC - 1 Hz to 50 kHz.

Differential Input

Input coupling: AC or DC, selectable.
Input impedance: 600 Ω or user supplied.
Sensitivity: 100 mV full scale to 10 V full scale (10 divisions in 1-2-5 steps).
DC accuracy: 100, 200, 500 mV full scale - ±0.5% of reading ±0.5 mV. 1, 2, 5, 10 V full scale - ±0.2% of reading ±0.1% of full scale range.
Resolution: 12-bits (0.024%) of full scale.
Position (DC offset): Adjustable over ±5 divisions with 12-bit resolution.
Maximum input voltage: ±12 V (DC + AC peak).
Large signal bandwidth: DC - 0 Hz to 60 kHz, AC - 120 Hz to 60 kHz.
Small signal bandwith (–3 dB points): DC - 0 Hz to 150 kHz, AC - 120 Hz to 150 kHz.
Reduced bandwidth using internal filter (–3 dB points): DC - 0 Hz to 4.8 kHz, AC - 120 Hz to 4.8 kHz.

Auxiliary Inputs

Input coupling: AC or DC, selectable.
Input impedance: 1 MΩ/25 pF.
Sensitivity: 5 V full scale.
DC accuracy: ±0.75% of full scale.
Resolution: 12-bits (0.024%) of full scale.
Position (DC offset): Adjustable over ±5 divisions

with 12-bit resolution.
Maximum input voltage: 10 V (DC + AC peak).
Large signal bandwidth: DC - 0 Hz to 50 kHz, AC - 1 Hz to 50 kHz.
Small signal bandwidth (–3 dB points): DC - 0 Hz to 425 kHz, AC - 1 Hz to 425 kHz.

Analog Trigger Input

Input coupling: AC or DC, selectable.
Input impedance: 1 MΩ/25 pF.
Sensitivity: 5 V full scale, AC+DC peak (x1). 50 V full scale, AC + DC peak (x10).
Maximum input voltage: 100 V (DC + AC peak).
Large signal bandwidth: DC - 0 Hz to 50 kHz, AC - 1 Hz to 50 kHz.
Small signal bandwidth (–3 dB points): DC - 0 Hz to 425 kHz, AC - 1 Hz to 425 kHz.

Timebase (Time or Frequency Domain)

Horizontal sweep: 10 divisions in 1-2-5 sequence, 10 ms to 10 s/division, 10 kHz to 10 Hz/division, user defined sampling frequency or period.
Sample period resolution: 1 cycle of master clock (200 ns nominal).
Sample period range: 10 ms to 1 s/sample.
Sample frequency range: 100 kHz to 1 Hz.
Sample clock: Output - 1 Hz to 100 kHz (TTL levels, internal clock). Input - 1 Hz to 100 kHz (TTL levels, user supplied external clock).
Master clock: Internally generated 5 MHz clock, user supplied external master clock.
Mixed timebase: Runs after user defined number of samples of main timebase or externally switched via TTL input. (Not available in all modes of operation.)
Vernier delay (Trigger holdoff): Programmable in steps of master clock (0 to 65535).
FFT length: 64 to 1024 samples in binary sequence.
FFT window functions: Rectangle, Hann, Hamming, 3 term Blackman-Harris, 4 term Blackman-Harris.

Trigger - Analog

Sources: Internal (using signal derived from selected input. Range, ± full scale). External x1 (5 V full scale AC + DC peak), AC or DC coupled. External x10 (50 V full scale AC + DC peak), AC or DC coupled.
Resolution: 12-bits.
Accuracy: ±0.5% of full scale.
Bandwidth: DC - 0.1 Hz to 50 kHz, AC - 1 Hz to 50 kHz.
Internal and external analog trigger only. Measured using full scale sine wave as trigger signal, no offset, 0 V trigger point.

Trigger - Digital

Sources: Line (internally derived). Internal (Free run). External (TTL input), n-bits of an 8-bit TTL byte (1≤N≤8, individual bits and sense programmable. May also be used as a trigger qualifier). Cross trigger bus. Video line sync (line number selectable). Video field sync (even or odd field, PAL/NTSC system).

Trigger - General

Polarity: +ve or –ve slope, level or edge sensitive.
Output: Buffered TTL level.
Pre-trigger delay: Delay≤number of samples in trace, programmable up to 32768.
Post-trigger delay: ≤65536 x sample period or trigger events, programmable.
Arm signal: Internal or externally generated, TTL.
Holdoff: 0 to 10 ms in steps of one cycle of master clock.
Propagation delay: 100 ns, typical. (Measured from the rising edge of the external TTL trigger input to HOLD of analog waveform).

Acquisition Modes

Time domain: Single trace. Time averaging.
Envelope. (max/min hold over specified number of traces or continuous).
Frequency domain: Single trace. Frequency averaging (specified number of traces or continuous). Max hold (specified number of traces or continuous).
Display zoom: x1 to x128 in binary steps (horizontal only).
Cursors: Reference, measurement, position programmable.
Interactive: Interactive control of vertical and horizontal settings, magnification, display area, cursor positions and plot modes.

Waveform Generation

Amplitude: ±10 V max into 600 W, source resistance <1 Ω.
Resolution: 5 mV (12-bits of full scale value).
Accuracy: ±10 mV.
Clock source: Internal - 1 MHz maximum, 100 kHz.

default, 100 Hz minimum. External - 1 MHz maximum, 100 kHz default, 1 Hz minimum, TTL levels.

Timing resolution: Internal - 1 cycle of master clock. External - 1 cycle of external clock signal, ±200 ns. Frequency accuracy: As main timebase accuracy. DC level and offset: −10 V to +10 V.

Sine: Frequency - clock frequency ÷ 2^{16} to clock frequency ÷ 2. Frequency step size - better than clock frequency ÷ 2^{12}. Harmonics of full scale waveform (excluding clock related components) >40 dB down on fundamental.

Square: Frequency - clock frequency ÷ 2^{16} to clock frequency ÷ 2. Duty cycle - 0 to 1. (Minimum output pulse width is one clock cycle.)

Triangle: Frequency - clock frequency ÷ 2^{16} to clock frequency ÷ 2. Duty cycle - 0 to 1. (Minimum duration of each slope is one clock cycle).

Pseudo random noise: Peak level programmable.

User defined waveform: 1 to 32768 samples. If generation and sampling overlapped, maximum length is 32768 less sample length.

Waveform Memory
Memory size: 32768 x 16-bit words.
Sample record length: 32768 samples (16-bit words) maximum. Sample record length user selectable from 1 to 32768 words.
Reference waveforms: As sample record length.

DIGITAL MULTIMETER

■ A versatile instrument providing DC volts, AC volts and resistance measurement facilities and a current source

The Digital Multimeter (DMM) provides facilities for DC voltage, AC voltage and resistance measurement. The instrument card also contains a current source with five fixed outputs.

Specification

DC Volts – Ranges (Full Scale)/Resolution
±200 mV/0.05 mV.   ±200 V/50 mV
±2 V/0.5 mV.   ±350 V/500 mV
±20 V/5 mV.

DC Volts Accuracy
All ranges to 200 V: ±0.12% of reading, ±0.1% of range.
±350 V range: ±0.12% of reading, ±0.5% of range.

AC Volts – Ranges (Full Scale)/Resolution
200 mV rms/0.05 mV.   200 V rms/50 mV.
2 V rms/0.5 mV.   250 V rms/500 mV.
20 V rms/5 mV.

AC Volts Accuracy
All ranges to 200 V: ±1.2% of reading, ±1.22% of full scale.

Frequency Range
50 Hz to 50 kHz.

Input Impedance
10 MΩ in parallel with 50 pF.

Isolation
±350 V (DC + AC peak).

Resistance Ranges (Full Scale)/Resolution
200 Ω/0.05 Ω.   200 kΩ/50 Ω.
2 kΩ/0.5 Ω.   2 MΩ/500 Ω.
20 kΩ/5 Ω.   20 MΩ/5 kΩ.
20 MΩ/5 kΩ.

Resistance Accuracy
200 Ω range: ±0.35% of reading, ±0.3% of range.
2 kΩ, 20 kΩ and 200 kΩ ranges: ±0.35% of reading, ±0.1% of range.

Current Sources (Fixed Outputs)
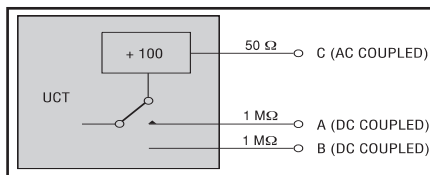100 nA, 1 mA, 10 mA, 100 mA and 1 mA.

Current Source Accuracy
±1%.

UNIVERSAL COUNTER TIMER

■ A multi-channel instrument which supports a wide range of measurement functions up to 150 MHz

The Universal Counter Timer (UCT) provides facilities for frequency measurement, period, time interval measurement, event counting and frequency ratio measurement.

UCT Configuration

The UCT is a two-channel (A & B) instrument operating to 10 MHz on-channel and 2.5 MHz between channels A and B. A 'third channel' operates from 10 MHz to 150 MHz with an input impedance of 50 Ω acting as a 100:1 pre-scaler.

Programmable attenuators are provided on channels A and B allowing input levels of up to 30 V peak. DC coupling is provided, with provision for input offset of up to 25 V.

Specification

Frequency Measurement
Range   DC to 150 MHz.

Period Measurement
Range   500 ns to 10 s with averaging.

Time Measurement
Range   500 ns to 10 s.

Event Counting
Range   DC to 10 MHz.
                 Up to 10 million counts.

Input Impedance
Channels A & B   Dual 1 MΩ inputs, DC coupled.
Channel C   50 Ω pre-scaler, AC coupled.

Inputs
Threshold   Up to 30 V peak.
Trigger level   Up to 24 V.
Resolution   Down to 20 mV.

Timebase Accuracy
10 ppm ±0.5 ppm

GENERAL PURPOSE SIGNAL ROUTING CARD

■ Software controlled
■ Supports VXI and GPIB external instrumentation

A function card which provides a combination of matrix and tree switching facilities for general purpose signal routing between internal or external instruments/resources and UUTs.

The General Purpose Signal Routing Card (GPSR) provides software controlled interconnections between the UUT, other configured ATE test resources and external instrumentation including GPIB or VXI controlled facilities. The card provides connections to/from the test fixture, the in-circuit analog bus (ICAB) used on the universal in-circuit test resource and an external I/O connector.

Features
• Eight single pole I/O relays.
• Two, 1:4 mux groups.
• Four, 1:2 mux groups.
• Connection of ICAB, via isolating relays to the test fixture.
• Connection of ICAB to 6 X 8 matrix, which permits routing to the ATE pinface or external I/O.
• Two poles of the 2:8 mux pairs with 200 V isolation characteristics.
• Sixteen I/O pairs, relay isolated, between external I/O and pinface.
• Six pseudo "twisted pair" I/O connections for low noise or controlled impedance applications.

External I/O and ICAB Connectors
In addition to the ATE system pinface connector, the card contains two external connectors. One 40-way connector provides access for external input/output resources and the second, a 16-way, provides access to the in-circuit analog bus used on the universal in-circuit test resource.

The 40-way header connector provides connection to all external I/O lines/user facilities. Some lines are tracked on the GPSR card as pseudo "twisted pairs" with their associated return path. The characteristic impedance of this tracking is approximately 100 Ω and can be used in low noise or controlled impedance applications.

The 16-way header connector pinout matches that of the DAS/UTP and ICR69 card and can be used to connect to the ICAB. By 'extending' the ICAB in this way means that access can be gained to any test point on the in-circuit pinface. Alternatively, this can be used as a general purpose 6-wire highway.

The ICAB lines can also be routed via a 6 X 8 matrix which will take any of the 6-wire bus lines and connect them to any of the eight external I/O lines. These in turn can be connected to the pinface.

The external I/O connector provides access to sixteen signal pairs which can be routed via double pole isolating relays to the pinface. Also access, via isolating relays, to the common line of each of the 2-way and 4-way MUX groups.

Two signal pairs from the external I/O connector can be routed via an 8 X 2 Pairs MUX to the pinface.

On 5305, a ribbon cable connector is provided on the rear breakout panel. It can

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be used for connection to the GPSR 40-way connector for external I/O routing.
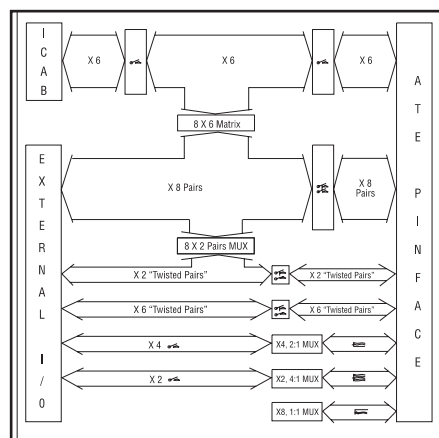
GPSR Block Diagram

Specification

Voltage Switching Capability
100 V DC or AC peak.
(200 V DC or AC peak for 2:8 MUX pairs.)

Current Switching Capability
0.5 A.

Power Switching Capability
10 W.

Carry Current
1 A.

Path Resistance
External I/O to pinface : 0.5 Ω max.
MUX I/O to MUX I/O : 0.6 Ω max.
MUX I/O to common : 0.8 Ω max.

Isolation Voltage
100 V DC or AC peak.
(200 V DC or AC peak for 2:8 MUX pairs.)

Bandwidth
10 MHz.

GENERAL PURPOSE RELAY CARD

- ■ Provides power and signal switching
- ■ Software controlled
- ■ Switchable for external instrumentation

Two cards providing software controlled interconnections between the Unit Under Test (UUT) and instrument or function cards.

The General Purpose Relay card provides software controlled interconnections between the UUT and instrument or function cards. Two versions of the GPR are available:-
- Dry reed switching card (GPR[D]).
- Mercury wetted relay switching card (GPR[W]).

The mode of operation is similar and the hardware of each type differs only in the type of relays fitted.

Each GPR card contains 32 individually-controllable relays arranged in eight groups, each group consisting of a 1 x 4 matrix. The relays are capable of switching analog signals or power to parts of a circuit

under test.

Software support for symbolic variables is provided enabling multiple relay operations. The choice between the use of a GPR(D) or a GPR(W) card depends on the nature of the loads/signals to be switched and the switching characteristics.
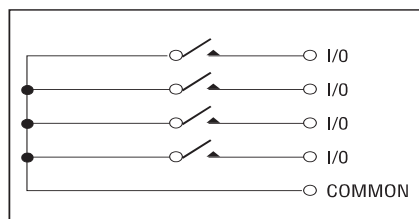
GPR Relay Group

Specification

Voltage Switching Capability
150 V DC or AC peak.

Current Switching Capability
GPR(D): 0.75 A.
GPR(W): 1 A.

Power Switching Capability
GPR(D): 10 VA.
GPR(W): 50 VA.

Carry Current
2 A DC or AC rms.

Frequency Range
DC to 10 MHz.

Open Switch Isolation
Not less than 125 MW.

Isolation Voltage
150 V DC or AC peak.

TELEPHONE TEST SUITE

A suite of cards providing line interface, ringing supply, dialling and acoustic interface facilities for testing telephones and their associated PCBs.

The telephone test suite of cards consists of the following four dedicated cards for telephone printed circuit board and telephone testing.

- Telephone Line Interface Card (TLI)
- Telephone Ringing Supply Card (TRS)
- Telephone Dialling Card (TDC)
- Telephone Acoustic Interface Card (TAI)

To complete the stimulus, measurement and switching requirements for both telephone printed circuit cards and complete telephones additional cards are required from the standard range of 5300 series test resource cards.

These are as follows:

- Waveform Synthesizer Card (WSC)
- Digital Multimeter Card (DMM)
- Analog Sampling Card (SAM[HR])
- General Purpose Relay Card (Dry Reed or Mercury Wetted Relays) (GPR[D] or [W])

The TLI card connects the telephone or associated PCB under test to the ATE and provides all of the switching required for

the waveform source and measurement instruments.

The TRS card provides a ringing supply and a constant current source. The frequency and amplitude of the ringing signal can be programmed or preset values may be used. A set of four presets allow different combinations of frequency and amplitude to be set up on the card. The output is differential from the transformer output stage. The constant current source output current can be set to four preset currents for recall by software as required. A programmable current is also provided. The source is powered from an external 48V supply normally (up to 60V maximum) and is isolated from the ATE 0V.

The TDC card provides a facility for testing the dialling functions. It provides a tone detection and analysis circuit for tone dialling. The detection facility consists of circuitry which can detect a valid DTMF tone and signal the digit dialled. The circuitry provides tone separation so that the level and frequency of each tone can be measured. Sequences of digits can be detected to test telephone memories and last number redial up to 40 digits.

A measurement facility is provided to detect a dialled digit from a telephone under test.

The card can measure a large number of parameters for dialling including make time, break time, make voltage, break voltage, IDP, make current, break current etc. Sequences of digits can be detected to test telephone memories and last number redial up to 40 digits.

The TAI card provides three microphone pre-amplifiers. The amplifiers provide an interface between external microphones to a DMM or SAM(HR) card for measurement. The amplifier gains are user preset via potentiometers to allow calibration against external instruments.

Specification

TELEPHONE LINE INTERFACE CARD

Telephone Feed Characteristics

Types	Voltage and current.
Voltage Source	30-60 V, programmable
Polarity	Normal & reversed, programmable.
Feed impedances	DC Direct. DC via 400 Ω. DC via 1500 Ω. DC via 1900 Ω.
Constant Current Source	
Current	5mA to 125 mA, fully software programmable or user preset-able currents selected by programming.
Voltage limit	30-60 V.
Line interface	
Telephone line impedances are programmable as follows.	
High impedance	>200 kΩ.
600 Ω	600 Ω resistive load.
ZREF1	370 Ω + 620 Ω in parallel with 310 nF ZREF (UK).
ZREF2	220 Ω + (820 Ω in parallel with 115 nF).
Ring load	800 Ω + 3 μF.
Balance load	300 Ω + 300 Ω + center tap.
Short circuit	2 Ω.
Coupling	DC coupling to loads: 2 μF + 2 μF capacitor in A and B lines (Non polarised).

5300 series

	220 µF + 220 µF capacitors in A and B lines (Polarised electrolytic).
Line simulators	0 km, 0.5 km, 7.0 km, 7.5 km & external.

TELEPHONE RINGING SUPPLY CARD

Voltage	10-100 V rms.
Resolution	Better than ±1 V rms.
Accuracy	Better than ±2 V rms, ±2% of value.
Frequency	20-25 Hz at 10-80 V, programmable. 25 Hz at 10 V-100 V, programmable.
Resolution	Better than 1 Hz.
Accuracy	Better than ±2 Hz, ±2% of value.
Cadencing	2 ON and 2 OFF times, presettable.
Range	Programmable from 1ms to 999 ms.
Accuracy	Better than ± (5 ms+5% of value).
series	Direct, 1500 Ω, 5100 Ω, resistance 6600 Ω.

TELEPHONE DIALLING CARD

Pulse (Loop Disconnect) Dialling Measurement

Pulse measurement	Up to 1999 ms.
Make, break accuracy	Better than 0.1 ms.
Volts accuracy	Better than 100 mV.
Inter digit pause (IDP) time	2000 ms max.
IDP accuracy	Better than 0.1 ms.
Sequence length	40 digits maximum.

DTMF Dialling Measurements

Tone Splitting Using TDC Card	
Frequency accuracy	Better than 0.1%.
Amplitude accuracy	± 0.5 dBm.
IDP time	1-1999 ms.
IDP accuracy	Better than 3 ms.
Accept frequency	Within 2.5% of nominal.
Reject frequency	Greater than 3.5% from nominal.
Minimum tone duration	30 ms.
Max. allowable dropout	20 ms.
Max. allowable twist	±10 dB.
Memory testing	40 digits maximum.
Fourier Analysis Using SAM(HR) Card	
Frequency accuracy	Better than 0.1%.
Amplitude accuracy	±0.1 dBm.
Twist accuracy	±0.1 dB.
Tone duration	Better than 1 ms.
IDP time	1-1999 ms.
IDP accuracy	Better than 1 ms.

TELEPHONE ACOUSTIC CARD

Acoustic Interface	
Loudspeaker Drive	
No of interfaces	2.
Gain	Presettable.
Total maximum power	2 W.
Loudspeaker impedance	8 Ω Minimum.
Microphone Interface	
No. of interfaces	3.
Gain	Presettable.
Typical microphone Z	600 Ω nominal.
Microphone power	0-10 V DC adjustable by preset.

ISDN TEST SUITE

■ Key layer 1 test facilities at all interfaces

■ Data link setup control (layer 2) and basic call setup functions (layer 3)

■ Protocol standards include EDSS1, VN4 and customized versions

■ Direct programmable access to B-channel data for Bit Error Rate testing

The ISDN test suite consists of a number of cards which provide the functional hardware and software to test S-interface and U-interface (Basic Rate) and S(2M) (Primary Rate) ISDN equipment at layers 1, 2 and 3 of the OSI reference model.

The key layer 1 test features include activation/de-activation, pulse shape verification and INFO signal debug. The latter provides time-stamping and event sequence checking of the activation/deactivation processes. Pulse shape verification enables checking that a pulse on a specific interface is within the defined limits.

Layer 2 and 3 testing includes D-channel protocol handling for basic call setups to CCITT or AT&T standards. Non-standard D-channel protocols can also be programmed to provide analysis and debugging of the D-channel data transfer.

Direct access to B-channel data is available with the ability to re-route it to other ATE system test resources – for example for digital-to-analog or analog-to-digital testing of an ISDN telephone, the B-channel can be routed to the ATEs SAM(HR) [High Resolution sampling card] which can provide both analog and digital data generation and analysis. A-law and µ-law encoding/ decoding is available. In the case of completely digital products, B-channel bit error rate testing can also be performed.

Test configurations for interface power consumption, voltage reversal, phantom power feed characteristics are provided.

Features

- Activation/de-activation (Layer 1)
- Pulse mask comparison
- Power feed characteristics
- Power consumption characteristics
- Data link setup control (Layer 2)
- Basic call setup functions AT&T, CCITT (Layer 3)
- Incoming call / Outgoing call setup
- Info analysis/time stamping
- Customized D-channel protocol facilities
- B-channel access
- BERT testing of B-channels
- B-channel loopback facility
- External line simulator access

ISDN Control Card

The ISDN Control (ISDNC) card provides the protocol handling for layers 1, 2 and 3. Activation/ de-activation functions are held in EPROM and actioned by one of the three resident microprocessors.

Higher level protocols are handled by either hardware or firmware. Programming facilities to enable customizing protocols are available. Clock circuitry and control is provided for the ISDN Load card via a standard interface. Provision has also been made for accepting external

synchronization, a programmable gate array design provides the ideal flexibility for dealing with a variety of test configurations.

The B and D-channels can be routed to different functions on board plus interfaced directly to other ATE resource cards. When performing A/D, D/A half channel tests, the SAM(HR) card can provide the digital data generation and measurement for the 64 kbit/s data stream from a B-channel. Clocks and timing are sourced by the ISDN Control card. Similarly, if a BERT test is being performed, the B-channel data can be accessed by one of the on board micro-processors and suitable error checking or data verification actioned.

The D-channel data is automatically stored for analysis either during program run time, or at a later time during program generation debug. Similar facilities are available for analyzing the activation and de-activation functions; 'INFO' states can be time stamped and the sequence checked for correct operation.

Interface Cards

The interface to the ISDN lines is provided by various ISDN Load cards, each with the associated test and termination loads fitted. One card (ISDNS) is of the S-interface type, and three cards (ISDNU-2B1Q, ISDNU-Up0 and ISDNU-4B3T) are of the U-interface type. Switching, buffering and routing of signals to other ATE test resources for parametric tests are available under high level software control.

A programmable supply path with reversal relays, power feeding transformers and current consumption measurement facilities can be utilised, the ATE's internal user supply being the power source. Switching is available for adding in external loads or external line simulators.

Together with the ISDNC card, the interface cards can be configured, under program control, to interface to the various ISDN configurations TE, NT and LT equipment.

When testing ISDN linecards, extra load cards could be added to the system (up to four per ISDNC card) to test channels in parallel.

High Speed Sampling

To perform the ISDN parametric tests at layer 1, the ISDN test facilities requires a high speed sampling facility. This test resource is provided by the SAM(HS) card which can capture and analyze the ISDN interface waveforms, perform mask generation, waveform measurement and analysis.

Applications

The following is a set of examples of ISDN test solutions provided by IFR

S-Interface ISDN phone.

Specified Tests:-

- Simulation of NT side
- Activation / Deactivation
- Overlap outgoing call setup
- Key press verification
- En Bloc outgoing call setup
- Incoming data call setup

- Rx Sensitivity (including BERT)
- S pulse mask test

S/U-2B1Q Interfaces ISDN Network Termination Unit

Specified Tests:-

- Simulation of LT and TE.
- Activation / Deactivation
- Wiring Polarity Integrity
- S and U pulse shape
- U Total power
- Maximum range (BERT over U line length max.)
- Return Loss
- Current Feed

S/U-4B3T Interfaces ISDN Network Termination Unit

Specified Tests:-

- Simulation of LT and TE.
- Activation upstream/ downstream
- Deactivation
- S-interface voltage measurement
- Current limit tests - for various loads on S-interface.
- BERT over U maximum line length.
- S-interface emergency power

U-2B1Q Interface ISDN Line Termination Unit

Specified Tests:-

- Simulation of NT and PCM 2M interface.
- Activation / Deactivation
- Wiring Polarity Integrity
- Power feed loading
- U pulse shape
- U Total power
- Maximum range (BERT over U line length max.)
- Return Loss
- Current Feed

PABX Testing

Interfaces tested:-

- Analog (voice)
- S (Basic rate)
- T (Basic rate)
- Up0 (Basic Rate)
- S(2M) Primary rate

Specified Tests:-

- Activation / Deactivation (layer1)
- Data link setup (layer2)
- Call setups - Incoming and Outgoing.
- BERT - both B channels simultaneously.

Call setup combinations:-

- S ↔ S, S↔ Analog
- T↔ S, T↔ Analog
- S (2M) ↔ S, S(2M)↔ Analog
- Up0 (DECT)↔ S

Protocols used:-

- EDSS1, VN4 over S and S(2M).
- Proprietry over S.
- DECT proprietry over Up0 interface.

Primary Rate Interface Testing

A configuration using the ISDNC, TDI & PEC provides a solution for interfacing to the ISDN Primary rate (2M) interface.

Specification

S (B23514)

S-bus Interface Input
AMI to I.430, 2B+D channels, 2-wire.

S-bus Interface Output
AMI to I.430, 2B+D channels, 2-wire.

Loads
No load, 5.6 Ω, 100 Ω, 400 Ω. Power load 200 Ω/2 Ω and external.

Terminations
Termination resistor 100 Ω and no termination.

Line Simulator
Switched access for external line simulator.

Buffer Amplifier
X1 and X10.

Switching
DC power routing for UUT and current monitoring.

U-2B1Q (B23512)

Interface
U, 2-wire to ITU G961.

Linecode
2B1Q.

Channels
2B + 1D.

Loads
No load, 135 Ω , 135 Ω balanced, AC/DC coupling.

Power Load
2 x 4k7 2W.

Termination
135 Ω, no termination.

Line simulator
Switched access for external line simulator.

Buffer Amp.
X1 and X10.

Switching
DC power routing for UUT, voltage and current monitoring.

Up0 (B23516)

Interface
U, 2-wire Half-duplex burst mode ("ping-pong")

Linecode
AMI

Channels
2B + 1D.

Loads
No load, 100 Ω , 100 Ω balanced, AC/DC coupling.

Power Load
2 x 4k7 2W.

Termination
100 Ω, no termination.

Line simulator
Switched access for external line simultor.

Buffer Amp.
X1 and X10.

Switching
DC power routing for UUT, voltage and current monitoring.

U-4B3T (B23517)

Interface
U, 2-wire to FTZ Guideline 1 TR 220

Linecode
4B3T

Channels
2B + 1D.

Loads
No load, 150 Ω , 150 Ω balanced, AC/DC coupling.

Power Load
2 x 4k7 2W.

Termination
150 Ω, no termination.

Line simulator
Switched access for external line simultor.

Buffer Amp.
X1 and X10.

Switching
DC power routing for UUT, voltage and current monitoring.

ISDNU-2B1Q INTERFACE CARD

2B1Q- B23512/2

This card is used to interface to the ISDN 2-wire U-2B1Q interface (ITU G691). It is configurable either as a network terminator (NT) or as a line terminator (LT).

The U-interface features are controlled via the IOM interface by the ISDNC card which routes B and D channel data to and from the U-interface. The other load and test features of the card are controlled via the 5300 interface.

The 2B1Q card provides a number of loads and terminations for various test configurations and parametric tests on the U-interface. This includes both phantom and normal power feed facilities. Stimulus and measurement paths are used to route signals to and from the other instrumentation cards in the 5300 system.

The card consists of the following functional blocks :

- U-interface circuitry
- Power feed circuitry
- Termination and measurement loads
- Differential to single-ended amplifier buffer
- Line simulator access

U-Interface Circuitry

The U-interface contains a 15.36 MHz crystal for a local clock source, and a phase locked loop circuit to synchronize with the incoming 2B1Q signal. It also contains line conditioning components and the interface transformer, which can provide a DC phantom voltage feed.

The U-interface circuitry can be isolated from the rest of the card under software control.

Power Feed Circuitry

This takes an external voltage supply from the pinface and routes it either as a phantom feed over the U-interface or as a power source_2 via the pinface. The circuitry can also provide voltage reversal, in-line chokes, current monitoring resistor and internal and external feed loads. Connections from suitable monitoring points can be routed to a single pair of wires on the pinface for onward routing to, for example, the system DMM.

Termination and Measurement Loads

The power feed and the U-interface transceiver circuitry are routed into the 2-wire test bus load block which provides both terminations and test loads. The DC termination can be 135 Ω or open circuit, and the AC termination can be either 135 Ω or a balanced 135 Ω in the U test

5300 Series

bus block.

The card also contains balanced loads and a return loss bridge required for measuring Longitudinal Conversion Loss and return loss.

Amplifier Buffer

The differential signal of the U-interface has to be conditioned before routing to single-ended measurement instruments in the M5300. This amplifier buffer can do this. It has a x1 and X10 gain setting for improved resolution for performing parametric gain measurements.

Line Simulator Access

An external line simulator can optionally be inserted in the signal path of the U-interface test bus. Connections are made at the pinface. Alternatively the same connections can be used for the insertion of a line attenuator.

Specification

Maximum phantom supply feed rating
60 mA

Maximum termination resistance rating
0.5 W

MATRIX SWITCH CARD

MSC - B23108/2

The Matrix Switching Card (MSC) contains two relay matrices, each of which is configured to provide a 16 x 4 selection.

The card can be configured to provide either two 16 x 4 matrices or one 32 x 4 matrix. The MSC cards bandwidth, isolation, switching capability and crosstalk performance make it ideally suited to most applications requiring a true matrix.

Specification

Bandwidth
20 MHz

Max Switching Voltage
200 V DC and AC peak

Max Switching Current
0.5 amp

Max Carry Current
1 amp

Max Switchable Power
10 VA per channel

PROTOCOL EMULATION CARD

PEC - B23540/2

The PEC card provides both serial and parallel interfaces capable of a wide range of uses for communications with UUTs.

The card contains a high performance, integrated multi-protocol processor (68302) incorporating three versatile serial communications controllers each independently capable of supporting UART, HDLC, BISYNC and DDCMP modes or variants of these.

The digital interface provides 16 parallel

drive / sense lines with input / output protection. The serial interface facility supports RS232C, RS422A, V10, V11 and TTL level interfaces. The telecommunications highway comprises 3 x RS485 bi-directional links for inter-connecting with ISDN and telecommunications data interface test resources.

Hardware Features

- High performance Motorola 68302 Integrated Multi-protocol Processor (IMP) running at 16.384 MHz.
- IMP incorporates 3 versatile Serial Communications Controllers (SCC's) each independently capable of supporting UART, HDLC, BISYNC and DDCMP modes or variants of these. Some ISDN functions including rate adaption to V.110 are also supported.
- Memory includes 256 kbytes ROM and 1 Mbyte RAM with 0 wait state operation. There is also 32 kbytes of RAM for interfacing to the ATE system.
- Serial Interface System supports RS232, V10, V11 and TTL level interfaces independent of SCC protocol selected.
- Telecommunications highway comprising 3 x RS485 bi-directional links.
- Digital Interface with 16 parallel drive / sense lines with output / input protection.

Software Facilities

The software to control the PEC features are TPG based through profiles with the additional capability to store PEC information in disk files for fast re-load and execution.

Customization of the PEC is achieved by loading application specific information in the form of FPGA files and code overlays to support those interfaces not readily achieved with the standard features.

A single Xilinx FPGA site on the PEC supports 3042 type devices as standard. Larger scale FPGAs can be accommodated if required by customer applications.

INTERFACE LOGIC

RS-232C
Four outputs and four inputs which can be routed to any SCC. Maximum rate is 38.4 kbaud.

RS-422A
Four output pairs and four input pairs which can be routed to any SCC. Outputs have a global tri-state control, maximum rate 6.5536 MHz.

TTL
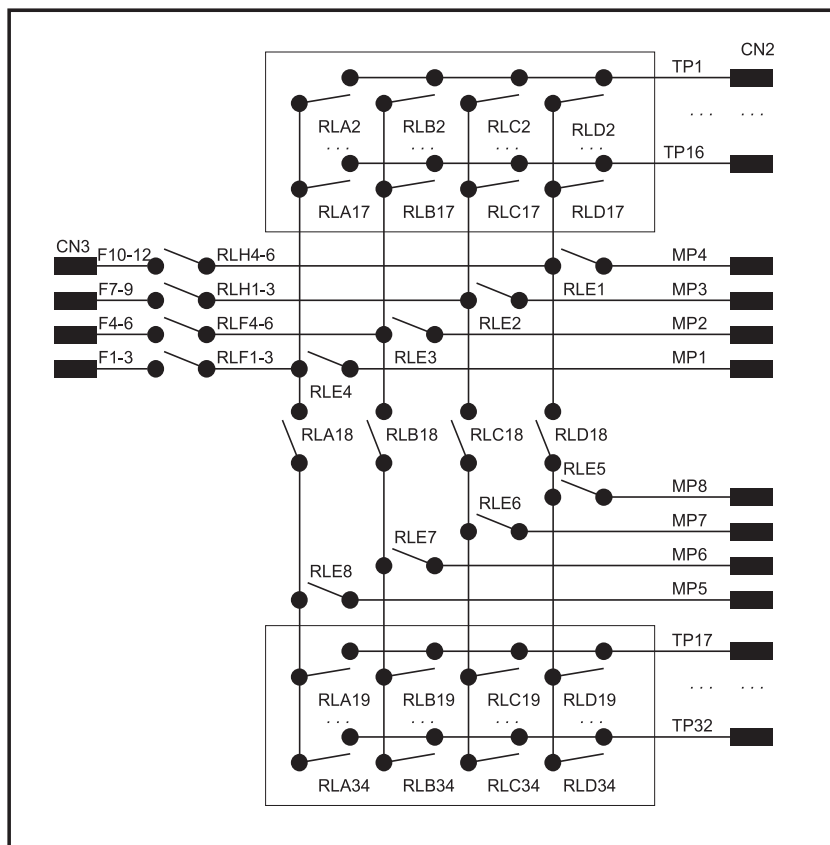Four outputs or four inputs in pairs. Each pair has a tri-state control, maximum rate is 6.5536 MHz.

RS-485
Three pairs for inter-instrument communication.

Parallel
16-bit I/O, low / high bytes have individual tri-state control.

Isolation
With the exception of the RS485, all interfaces are relay isolated.

MSC Card - Switching Diagram

MIL-STD-1553 BUS

1553 - B23087/2

The 1553B card allows the tester to interface with units under test which use the MIL-STD-1553 bus.

The card provides two data buses (BUS A and BUS B) via DIN 41612 mixed contact coaxial connectors. More than one card can be used in the tester.

The 1553B card DDC MIL-STD-1553 Advanced Integrated Mux (AIM) BUS-61553 hybrid device. This is a complete MIL-STD-1553 Bus Controller (BC), Remote Terminal Unit (RTU) and Bus Monitor (BM). It provides dual low power transceivers and complete BC / RTU / MT protocol logic, and MIL-STD-1553 to host interface unit and a fully memory mapped 8k x 16 RAM.

The card provides coupling transformers to both BUS A and BUS B and provision is made for direct coupling resistors on each bus.

Three modes of operation are available with the 1553 card. In all cases any response is stored for future comparison :

- Single, which transmits a single message or block of messages once.
- Run 'n' times, which transmits a single message or block of messages for a specified number of times.
- Continuous, which transmits a single message in a continuous loop and control is returned to TPG to continue execution of the main test program. A STOP command must be sent to halt the transmission. In this mode a replace command can be used to update a command or data word 'on the fly'.

Command messages can be written out in full, or loaded from predefined string arrays or downloaded from an external file containing arrays.

Specified words can be read back and compared individually (a data mask is available) or blocks of words can be loaded into a specified array.